WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Wednesday, January 26, 2005

Hide?	Set Name	Query	Hit Count
	DB=USPT; PLUR=YES; OP=ADJ		
☐	L4	L3 and (instruction near3 que$)	1
☐	L3	6049882.pn.	1
☐	L2	L1 near10 (power near (consumption or sav$))	1
☐	L1	(identif$ or monitor$ or determin$) near3 (instruction) near5 (pend$ or queu$)	550

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 6049882 A

L4: Entry 1 of 1 File: USPT Apr 11, 2000

DOCUMENT-IDENTIFIER: US 6049882 A
TITLE: Apparatus and method for reducing power consumption in a self-timed system

Detailed Description Text (12):
FIG. 8 shows an arrangement for adjusting power consumption for a self-timed processor according to a first preferred embodiment of the present invention. As shown in FIG. 8, a variable cycle time that is used to control power consumption is based on an instruction queue length. A power control device 802 dynamically adjusts the system performance (e.g., cycle time) and power consumption depending on work load requirements. In the first preferred embodiment, the system performance adjustment is achieved by changing a variable delay in one processing stage (e.g. instruction fetch).

Detailed Description Text (13):
As shown in FIG. 8, an instruction queue length is used to indicate the processor work load requirements. A counter is used to count the number of elements (e.g., instructions) waiting in a queue to be processed. The variable cycle time is then controlled by the power control device 802 as a function of queue length. As the "queue length" gets longer and there is more work to do, the delay (e.g., cycle time) is reduced. Accordingly, the system power consumption and system performance is increased. As the "queue length" of work becomes smaller, the cycle time is increased to decrease the power consumption and the system performance. Thus, power consumption corresponds to the amount of work (e.g., execution requirements of the processor) to be done.

Detailed Description Text (14):
Thus, in a self-timed system, the speed of operation can be controlled by controlling one part of the system. In FIG. 7, the cycle time of a sub-block or sub-system can be increased by increasing the delay in the handshake loop. Thus, the first preferred embodiment monitors instruction queue length to reduce power consumption of the self-timed system. Further, the control structure can be easily implemented.

CLAIMS:

3. The asynchronous system of claim 1, wherein the first and second operation speeds are determined based on at least one of instruction queue length, an instruction, an external signal and an application specific criteria.

5. The asynchronous system of claim 4, wherein the power control circuit selects the variable speed of operation based on at least one of instruction queue length, an instruction, an external signal and an application specific criteria.

6. The asynchronous system of claim 1, wherein the operating speed is a functional unit operation cycle time, wherein the cycle time is the inverse of a frequency of operation, and wherein the period of operation for the selected functional unit is proportional to an instruction queue length.

12. The data processing apparatus of claim 10, wherein a selected power level is based on at least one of instruction queue length, an instruction, and external signal and an application specific criteria.

25. The method of claim 19, wherein operating criteria are based on determining at least one of an instruction queue length, an instruction type, an external signal type and a functional unit type.

Terms	Documents
L3 and (instruction near3 que$)	1